

CLAIMS

What is claimed is:

1. A semiconductor device structure with a substantially planar surface, comprising:
a substrate including at least one recess formed therein; and
a material layer disposed over said substrate and substantially filling said at least one recess, said material layer having a substantially planar surface free of abrasive planarization-induced defects.

2. The semiconductor device structure of claim 1, wherein said substrate comprises a semiconductor substrate with a surface and said at least one recess comprises at least one trench recessed in said surface of said semiconductor substrate.

3. The semiconductor device structure of claim 1, wherein said material layer comprises a mask material.

4. The semiconductor device structure of claim 3, further comprising at least one conductively doped region continuous with a surface of said semiconductor substrate and laterally adjacent said at least one trench.

5. The semiconductor device structure of claim 1, wherein said substrate comprises:
a shallow trench isolation structure including a semiconductor substrate with a surface and at least one trench formed in said surface of said semiconductor device substrate; and
an insulator layer substantially filling said at least one trench and covering said surface of said semiconductor device substrate.

6. The semiconductor device structure of claim 5, wherein said insulator layer includes a nonplanar upper surface with at least one peak located substantially above said surface of said semiconductor device substrate and at least one valley located substantially above said at least one trench.

7. The semiconductor device structure of claim 6, wherein said material layer comprises a stress buffer layer that substantially fills said at least one valley in said insulator layer.

8. The semiconductor device structure of claim 1, wherein said substrate comprises: a semiconductor device structure including a surface with at least one dual damascene trench formed thereon; and a conductive layer substantially filling said at least one dual damascene trench and covering said surface of said semiconductor device structure.

9. The semiconductor device structure of claim 8, wherein said conductive layer includes a nonplanar upper surface with at least one peak located substantially above said surface of said semiconductor device structure and at least one valley located substantially above said at least one dual damascene trench.

10. The semiconductor device structure of claim 9, wherein said material layer comprises a stress buffer layer that substantially fills said at least one valley in said conductive layer.

11. The semiconductor device structure of claim 1, wherein said substrate comprises a stacked capacitor structure including an insulator layer with at least one container recessed therein.

12. The semiconductor device structure of claim 11, wherein said material layer comprises a mask material, said mask material substantially filling said at least one container.

13. The semiconductor device structure of claim 12, wherein mask material covering a surface of said insulator layer has a thickness of less than a height of said at least one container.

14. The semiconductor device structure of claim 12, wherein mask material covering a surface of said insulator layer has a thickness of less than about half a depth of said at least one container.

15. A semiconductor device structure with a substantially planar surface, comprising:
a substrate including at least one recess formed therein; and
a material layer disposed at least partially over said substrate so as to at least partially fill said at least one recess, said material layer having a substantially planar surface substantially free of abrasive planarization-induced defects.

16. The semiconductor device structure of claim 15, wherein at least one region of said substrate is exposed through said material layer.

17. The semiconductor device structure of claim 15, further comprising:
at least one intermediate layer between said substrate and said material layer, at least one portion of said intermediate layer at least partially filling said at least one recess.

18. The semiconductor device structure of claim 17, wherein at least one region of said at least one intermediate layer is exposed through said material layer.

19. The semiconductor device structure of claim 17, wherein said at least one intermediate layer comprises at least one of a mask material, an insulative material, and a conductive material.

20. The semiconductor device structure of claim 15, wherein said material layer has a thickness that is less than a depth of said at least one recess.